AMENDMENTS TO THE SPECIFICATION

Please replace paragraph [0007] with the following amended paragraph:

[0007] Please refer to Fig.1 of a schematic diagram of a prior ~~flash art~~ data converter 10, which is used to convert an analog input signal Vin to a corresponding digital signal. The data converter 10 comprises a voltage dividing circuit 12, an encoding circuit 16, and a plurality of comparison units 14. In Fig.1, eight comparison units are shown by way of example. The voltage dividing circuit 12 comprises a plurality of resistors such as Ra, Rb, and Rc for dividing a voltage Vdc into different reference voltages Vr1 to Vr8 respectively at each node. Each of the comparison units 14 comprises an amplifier 18 and a latch circuit 19. The amplifier 18 receives the reference voltage generated by the voltage dividing circuit 12, and an input signal Vin for amplifying the difference between these two input signals to generate a corresponding signal to the latch circuit 19. The latch circuit 19 is triggered by a clock vclock to convert the output signal of the amplifier 18 to a digital signal in a high or low state. This converted digital signal is output to the encoding circuit 16. The encoding circuit 16 processes (for example, corrects) and encodes the digital signals generated by the comparison units 14.

Please replace paragraph [0008] with the following amended paragraph:

[0008] Please refer to Fig.2 of a timing diagram of the clock vclock, the input signals Vin, and the output digital signals of each comparison unit while the prior art data converter 10 operates. The transverse axis in Fig.2 is time. When the analog input signal Vin reaches the data converter 10, the amplifier 18 compares the input signal Vin with the corresponding reference voltage and outputs a comparison result to the latch circuit 19. According to the comparison result and a trigger of the

clock vclock, the latch circuit 19 outputs a digital signal in a high state, which is shown by 1, or a low state, which is shown by 0. For example, at time t1, if the input signal Vin is less than the reference voltages Vr1 and Vr2 but more than the reference voltages Vr3 to Vr8, then the latch circuit 19 is triggered by the negative edge of the clock vclock (which is shown by arrows) and outputs digital signals as 0, 0, 1, 1, 1, 1, 1, and 1. In this manner, the input signal Vin at time t1 can be converted to a digital signal (0, 0, 1, 1, 1, 1, 1, 1). The encoding circuit 16 can encode the digital signal in advance, such as 011.

Please replace paragraph [0010] with the following amended paragraph:

[0010] To adjust for the offset voltage in the comparison units, an auto-zeroing process is used to solve the problem. Please refer to Fig. 3 of a schematic diagram of a data converter 20 in the prior art. The data converter comprises a voltage dividing circuit 22 for providing reference voltages Vr1 to Vr4, four comparison units 24A to 24D, auxiliary circuits 26A and 26B, and an encoding circuit 28. The comparison units 24A to 24D have the same structure. The comparison unit 24A comprises four switches SP1, SP2, SP3 and SP4, a differential amplifier Ka with one output end and two input ends, a capacitor C0, and a latch circuit Ja. The switches SP1 to SP4 are controlled by a control signal vc1 and an inverted signal of the control signal vc1, shown as $\overline{vc1}$.

The amplifier Ka comprises a feedback circuit controlled by the switch SP3 electrically connected to the input end P11 and the output end P12. The other input end of the amplifier Ka is electrically connected to a common mode voltage V0. The latch circuit Ja is triggered by the clock vclock. Each comparison unit is electrically connected to a resistor Rc.

Please replace paragraph [0022] with the following amended paragraph:

[0022] It is an advantage of the claimed invention that the comparison units of one set are performing auto-zeroing, and the comparison units of the other set perform the data conversion to generate corresponding digital signals ~~simultaneously. In~~ simultaneously. In addition, the active interpolation in the claimed invention simplifies the circuit layouts so that the design and manufacturing time and costs are reduced. Moreover, result achieved by the active interpolation in the claimed invention is less sensitive to the non-linear characteristic of the converting curves.

Please replace paragraphs [0047]-[0052] with the following amended paragraphs:

[0047] Please refer to Fig.12, which is a schematic diagram of a second data converter 60 according to the present invention. The data converter 60 is an analog to digital data converter that performs in a differential manner. In another words, the data converter 60 converts a difference of two analog input signals, which are Vin+ and Vin-, to digital signals such as digital bits. The data converter 60 comprises a voltage dividing circuit 62, a plurality of comparison units 64a, 64b, 64c, 64d, and an output unit 66. Please note that only four comparison units 64a, 64b, 64c, 64d are shown in Fig.12. However, the total number of comparison units used in the data converter 60 according to the present invention is not limited. To operate in a differential manner, the voltage dividing circuit 62 generates reference voltages Vr1a, Vr2a, ~~Vr1b, and~~ Vr1b, and Vr2b

via resistors and biased circuits 63A and 63B. Since the voltage dividing circuit 62 is similar to those in the prior art, it should require no further description.

[0048] Each comparison unit has the same structure. For example, the comparison unit 64b comprises eight switches S1 to S8 which are controlled by control signals AZ1, Az, and AZ2, wherein the switches in the comparison units 64A and 64C are controlled by control signals AZ1a and AZ2a and an inverted signal of Az. The comparison unit 64b also comprises a differential amplifier Qb comprising two differential input ends, a positive output end and a negative output end. In addition, the amplifier Qb comprises two feedback circuits controlled by switches S5 and S6 respectively. Both input ends are electrically connected to capacitors C. The other ends of the capacitors C are controlled by switches S3, S4 and are electrically connected to a reference voltage or an input signal, alternatively. The switches S1, S2 are used to control if reference voltages Vr1a, Vr1b are inputted into the comparison unit 64b, and the switches S7, S8 are used to control if the positive output end and the negative output end of the amplifier Qb are electrically connected to input nodes IN3, IN4 of the output unit 66. As shown in Fig.12, a positive output end and the negative output end of an amplifier Qa are controlled to be electrically connected to input nodes IN1, IN2; a positive output end and a negative output end of an amplifier Qc are controlled to be electrically connected to input nodes IN5, ~~IN6;finally~~ IN6; finally, a positive output end and a negative output end of the amplifier Qd are controlled to be electrically connected to input nodes IN7, IN8.

[0049] Please refer to Fig.13, which is a schematic diagram of the output unit 66 shown in Fig.12. The output unit 66 includes an interpolating unit 68, a plurality of latches 70a, 70b, 70c, 70d, 70e, and encoding logic 72. The interpolating unit 68 has three differential

amplifiers Q1, Q2, Q3, and each of the differential amplifiers Q1, Q2, ~~Q3has~~ Q3 has two pairs of differential input ends, a positive output end, and a negative output end. The latch 70a is used for latching a digital bit b1 associated with either the comparison unit 64a or the comparison unit 64b according to a clock ~~Vp.Similarly~~Vp. Similarly, the latch 70e is used for latching a digital bit b5 associated with either the comparison unit 64d or the comparison unit 64c according to the same clock Vp. In addition, the latches 70b, 70c, 70d are respectively used for latching digital bits b2, b3, b4 associated with the differential amplifiers Q1, Q2, Q3. For matching the differential output of the amplifiers Qa, Qb, Qc, Qd, Q1, Q2, ~~Q3,each of thelatches~~ Q3, each of the latches 70a, 70b, 70c, 70d, 70e also works in a differential manner. For example, if the input at node ~~Aof~~ A of the latch 70a is larger than the input at node B of the latch 70a, the latch 70a outputs the digital ~~bitb1~~ bit b1 that corresponds to a high logic level. In the same manner, a low logic level is assigned to the digital ~~bitb1~~ bit b1 if the input at node B is larger than the input at node A. In the end, the encoding logic 72 generates a digital value based on the received digital bits b1, b2, b3, b4, b5.

[0050] Please refer to Figs.11 and 12 in conjunction with Fig.7. The second data converter 60 operates according to the timing diagram shown in Fig.7. If a control signal corresponds to the high logic level, a switch controlled by the control signal is switched on to transfer signals. On the other hand, if the control signal corresponds to the low logic level, the switch controlled by the control signal is switched off to block signals from being transmitted. As shown in Fig.7, the control signals Az, AZ1a, ~~AZ2aat~~ AZ2a at time t3 correspond to the low logic level, but the controls signals AZ1, AZ2 correspond to the high logic level. Therefore, the comparison units 64b, 64d are in the auto-zeroing process, and the comparison units 64a and 64C are in the comparing process. At this time, the switches controlled by the control signal AZ2a are opened and do not establish the feedback paths for the amplifiers Qa, Qc.

Because the control signal AZ corresponds to the high logic level, the capacitors C are electrically connected to the input signals Vin+ and Vin-.

[0051] With regards to the amplifier Qa, the differential input signals Vin+, ~~Vin-are~~ Vin- are compared to the reference voltages Vr1a, Vr1b previously stored by the capacitors C, and corresponding signals output from the positive output end and the negative output end are further transmitted to the input nodes IN1, IN2 of the output unit 66. With regard to the amplifier Qc, the differential input signals Vin+, ~~Vin-are~~ Vin- are compared with to reference voltages Vr2a, Vr2b previously stored by the capacitors C, and corresponding signals output from the positive output end and the negative output end are further transmitted to the input nodes IN5, IN6 of the output unit 66.

[0052] When the signals output from the amplifier Qa are transmitted to the latch 70a, the latch 70a latches the digital bit b1 in the above-mentioned differential manner. Similarly, the latch 70e also latches the digital bit b5 in the above-mentioned differential manner when the signals output from the amplifier Qc are transmitted to the latch 70e. It is obvious that comparison units Qa, Qb, Qc, ~~Qdare~~ Qd are divided into two groups arranged in an interlaced manner. At the same time, half of the comparison units perform the auto-zeroing process and the other half performs the comparing process. In the preferred embodiment, an active interpolation is performed so that the interpolating unit 68 is capable of generating the digital bits. The operation of the active interpolation is described as follows. Please refer to Fig.14, which is a schematic diagram of converting curves of the comparison ~~unitsshown~~ units shown in Fig.12 and Fig.13. The transverse axis shown in ~~Fig.14represents~~ Fig.14 represents differential input voltages. The longitudinal axis shown in Fig.14 represents output voltages. The converting curve T1 represents a voltage conversion

characteristic for the signal output from the positive output end of the amplifier Qa, and the converting curve ~~T1"represents~~ T1' represents a voltage conversion characteristic for the signal output from the negative output end of the amplifier Qa. The converting curve ~~T2represents~~ T2 represents a voltage conversion characteristic for the signal output from the positive output end of the amplifier Qc, and the converting curve ~~T2"represents~~ T2' represents a voltage conversion characteristic for the signal output from the negative output end of the amplifier Qc. A voltage Vr1 marked on the transverse axis corresponds to reference voltages Vr1a, Vr1b. In the same manner, reference voltage Vr2 also corresponds to the reference voltages Vr2a, Vr2b. As described before, the intersections of the converting curves associated with the positive and corresponding negative ends correspond to the reference voltages in the transverse axis used to determine the digital bits latched by the corresponding latches. For example, if the differential input voltages Vin+, Vin- are greater than the reference voltage Vr1, the voltage level at the positive output end of the amplifier Qa is greater than the voltage level at the negative output end of the amplifier Qa according to the converting curves ~~T1, T1"~~T1, T1'. In other words, the voltage level at node B of the latch 70a is greater than the voltage level at node A of the latch 70a. Therefore, the digital bit is latched at the high logic level "1". On the other hand, if the differential input voltages Vin+, Vin- are less than the reference voltage Vr1, the voltage level at the positive output end of the amplifier Qa is less than the voltage level at the negative output end of the amplifier Qa according to the converting curves ~~T1, T1~~T1, T1'. In other words, the voltage level at node B of the latch 70a is less than the voltage level at node A of the latch 70a. Therefore, the digital bit is latched at the low logic level "0". Similarly, the digital bit b5 is also obtained according to the same process mentioned above.

Please replace paragraphs [0054]-[0057] with the following amended paragraphs:

[0054] In the preferred embodiment, each of the amplifiers Q1, Q2, Q3 corresponds to a specific voltage conversion characteristic through proper gain setting. With regard to the amplifier Q3, the amplifier Q3 amplifies the signal transmitted from the input node IN6 via a gain value equaling 3/4, and the amplifier Q3 amplifies the signal transmitted from the input node IN2 via a gain value equaling 1/4. Then, amplifier Q3 ~~superposesthese~~ superposes these two amplified signals to generate one differential output signal outputted from the positive output end. The converting curve T1 correspond to the signal transmitted by the input nodes IN6, and the converting curve T2 corresponds to the signal transmitted by the input node IN2. Therefore, the voltage conversion characteristic associated with the positive output end of the amplifier Q3 corresponds to the converting curve T3 shown in Fig.14 because of the executed interpolation process. Similarly, the amplifier Q3 amplifies the signal transmitted from the input node IN5 via a gain value equaling 3/4, and the amplifier Q3 amplifies the signal transmitted from the input node IN1 via a gain value equaling 1/4. Then, amplifier Q3 ~~superposesthese~~ superposes these two amplified signals to generate another differential output signal outputted from the negative output end. The converting curve T1 corresponds to the signal transmitted by the input nodes IN5, and the converting curve T2 corresponds to the signal transmitted by the input node IN1. Therefore, the voltage conversion characteristic associated with the negative output end of the amplifier Q3 corresponds to the converting curve ~~T3~~ T3' shown in Fig.14 because of the executed interpolation process. In addition, the intersection of the converting curves ~~T3, T3~~ T3, T3' corresponds to a reference voltage Vr3 interpolated between original reference voltages Vr1, Vr2.

[0055] With regard to the amplifier Q2, the amplifier Q2 amplifies the signal transmitted from the input node IN6 via a gain value equaling 2/4, and the amplifier Q2 amplifies the signal transmitted from the input node IN2 via a gain value equaling 2/4. Then, amplifier Q2

~~superposesthese~~ superposes these two amplified signals to generate one differential output signal outputted from the positive output end. Therefore, the voltage conversion characteristic associated with the positive output end of the amplifier Q2 corresponds to the converting curve T4 shown in Fig.14 because of the executed interpolation process. Similarly, the amplifier Q2 amplifies the signal transmitted from the input node IN5 via a gain value equaling 2/4, and the amplifier Q2 amplifies the signal transmitted from the input node IN1 via a gain value equaling 2/4. Then, amplifier Q2 also ~~superposesthese~~ superposes these two amplified signals to generate another differential output signal output from the negative output end. Therefore, the voltage conversion characteristic associated with the negative output end of the amplifier Q2 corresponds to the converting curve ~~T4~~ T4' shown in Fig.14 because of the executed interpolation process. In addition, the intersection of the converting curves ~~T4, T4~~ T4, T4' corresponds to a reference voltage Vr4 interpolated between original reference voltages Vr1, Vr2.

[0056] With regard to the amplifier Q1, the amplifier Q1 amplifies the signal transmitted from the input node IN6 via a gain value equaling 1/4, and the amplifier Q1 amplifies the signal transmitted from the input node IN2 via a gain value equaling 3/4. Then, amplifier Q1 ~~superposesthese~~ superposes these two amplified signals to generate one differential output signal output from the positive output end. The voltage conversion characteristic associated with the positive output end of the amplifier Q1 corresponds to the converting curve T5 shown in Fig.14 because of the executed interpolation process. Similarly, the amplifier Q1 amplifies the signal transmitted from the input node IN5 via a gain value equaling 1/4, and the amplifier Q1 amplifies the signal transmitted from the input node IN1 via a gain value equaling 3/4. Then, amplifier Q1 also ~~superposesthese~~ superposes these two amplified signals to generate another differential output signal output from the negative output end. The voltage conversion characteristic associated

with the negative output end of the amplifier Q1 corresponds to the converting curve ~~T5~~ T5' shown in Fig.14 because of the executed interpolation process. In addition, the intersection of the converting curves ~~T5, T5~~ T5, T5' corresponds to a reference voltage Vr5 interpolated between original reference voltages Vr1, Vr2.

[0057] From the above description, three reference voltages Vr3, Vr4, Vr5 are interpolated with proper gain setting designed for the amplifiers Q1, Q2, Q3 within the interpolating unit 68. It is obvious that the digital bits latched by the latches 70b, 70c, 70d are obtained by the active interpolation with the help of the amplifiers Q1, Q2, Q3. Please note that the amplifiers Qa, Qb have the same characteristics, and the amplifiers Qc, Qd have the same characteristics. Therefore, when the amplifiers Qa, Qc perform the comparing process, and the amplifiers Qb, Qd perform the auto-zeroing process, the amplifiers Qa, Qc, Q1, Q2, Q3 correspond to the converting curves shown in Fig.14. However, when the amplifiers Qb, Qd perform the comparing process, and the amplifiers Qa, Qc perform the auto-zeroing process, the amplifiers Qb, Qd, Q1, Q2, Q3 also correspond to the converting curves shown in Fig.14. In other words, ~~whenone~~ when one group consisting of comparison units 64a, 64c performs the comparing process, another group consisting of comparison units 64b, 64d then perform the auto-zeroing process. On the other hand, ~~whenone~~ when one group consisting of comparison units 64b, 64d performs the comparing process, another group consisting of comparison units 64a, 64c then perform the auto-zeroing process. In addition, the ~~latches70a~~latches 70a, 70b, 70c, 70d, 70e are triggered by the clock Vp to generate digital bits b1, b2, b3, b4, b5 according to the same reference voltages Vr1, Vr2 set by the voltage dividing circuit 62 and the reference voltages Vr3~Vr5 determined by the active interpolation. Therefore, the comparison units 64a, 64b correspond to the same voltage conversion characteristic, and the comparison units 64c, 64d correspond to the same voltage conversion characteristic as

well.

Please replace paragraph [0060] with the following amended paragraph:

[0060] In summary, the data converter of the present invention comprises a group of comparison units performing the auto-zeroing process and another group of comparison units performing the comparing process to generate corresponding digital signals and outputs of the comparison units performing the auto-zeroing process with an active interpolating manner. In contrast to the prior art, the data converter in the present invention offers several advantages. It is more flexible. The present invention uses an active interpolating manner so that the circuit structure is simpler and the resistor network is not required. Thus, time and cost for the designing and ~~manufacturingis~~ manufacturing is relatively reduced, and the operation is more precise. The problem of matching incorrectly is therefore also solved. The active interpolating manner in the present invention is less sensitive to the non-linear converting curves of the amplifier. The active interpolation used in the present invention only requires the converting curves of the positive and negative output ends of neighboring interpolating amplifier to be odd symmetric to each other and intersect at correct positions for the latch circuit to be driven in a differential manner. Thus, the requirement of the linear range of the converting curves in the present invention is lower than that in prior art.